WHAT IS CLAIMED IS:

1. An array substrate for use in an in-plane switching liquid crystal display device, comprising:

a plurality of gate lines disposed in a first direction on a substrate;

a plurality of data lines disposed in a second direction crossing the gate lines, wherein the gate and data lines have rounded portions and pairs of the gate and data lines define substantially circular pixel regions;

a common line disposed in the first direction between the pair of the gate lines;

a circular common electrode connected to the common line;

a thin film transistor disposed near each crossing of the gate and data lines; and

a circular pixel electrode disposed in the circular pixel region, connected to the thin film transistor, and spaced apart from the circular common electrode.

2. The array substrate of claim 1, wherein the pixel regions have a formation of delta structure where the pixel regions are distributed parallel from left to right and oblique from top and bottom.

3. The array substrate of claim 1, wherein the circular common electrode includes first and second substantially circular common electrode patterns, the first substantially circular common electrode pattern is larger than the second substantially circular common electrode pattern, and the second substantially circular common electrode pattern is inside the first substantially circular common electrode pattern.

4. The array substrate of claim 1, wherein the common line passes along a diametric line of the circular common electrode such that the common line divides the circular common electrode in two semicircular portions.

5. The array substrate of claim 3, wherein the circular pixel electrode includes

first and second circular pixel electrode patterns, the second circular pixel electrode pattern is disposed inside the second circular common electrode pattern, and the first circular pixel electrode pattern is disposed between the first and second circular common electrode patterns.

6. The array substrate of claim 5, further comprising a pixel connecting line connects the first and second circular pixel electrode patterns.

7. The array substrate of claim 6, further comprising a capacitor electrode over the first circular common electrode pattern, wherein the capacitor electrode is connected to the pixel connecting line, and the capacitor electrode and the overlapped portion of the first circular common electrode pattern constitute a storage capacitor.

8. The array substrate of claim 3, wherein the first circular common electrode pattern has an open corresponding to the thin film transistor.

9. The array substrate of claim 8, wherein the thin film transistor includes a drain electrode extends to the circular pixel electrode through the open of the first circular common electrode pattern.

10. The array substrate of claim 1, wherein the rounded portions of the gate and data lines correspond to the circular common and pixel electrodes.

11. An array substrate for use in an in-plane switching liquid crystal display device, comprising:

a plurality of gate lines disposed in a first direction on a substrate;

a plurality of data lines disposed in a second direction perpendicular to the gate lines, wherein the gate and data lines have a straight line shape and pairs of the gate and data lines define a rectangular pixel regions;

a circular common electrode disposed in each rectangular pixel region;

a common line disposed to the first direction, the common line connecting the circular common electrode to the neighboring circular common electrode disposed in the neighboring rectangular pixel region;

a circular pixel electrode disposed inside the circular common electrode with being spaced apart from the circular common electrode;

a thin film transistor disposed near a crossing of the gate and data lines in the rectangular pixel region; and

a pixel connecting line connecting the circular pixel electrode to the thin film transistor.

12. The array substrate of claim 11, wherein the circular pixel electrode has a circular band shape.

13. The array substrate of claim 11, wherein the circular common electrode has an open corresponding in position to the thin film transistor, and the pixel connecting line passes through the open.

14. The array substrate of claim 11, wherein the pixel connecting line does not cross the rectangular pixel region but cross over the gate line.

15. The array substrate of claim 11, wherein the circular common and pixel electrodes constitute a circular aperture area.

16. The array substrate of claim 1, wherein the pixel regions have a formation of straight structure where the pixel regions are distributed parallel both from left to right and from top and bottom.

17. A liquid crystal display device, comprising:

a plurality of substantially circular pixels disposed horizontally in at least adjacent first and second rows and vertically in at least adjacent first and second columns; and

pixels in the second row being offset in a horizontal direction from pixels in said first row by a predetermined distance.

18. The liquid crystal display device of claim 17, wherein the vertical distance between the first and second rows is less than the horizontal distance between first and second columns.

19. The liquid crystal display device of claim 18, wherein a top edge of a pixel in the second row is at the same vertical position as a bottom edge of a pixel in the first row.

20. The liquid crystal display device of claim 18, wherein a portion of a pixel in the second row is between two adjacent pixels in the first row.

21. The liquid crystal display device of claim 17, wherein a first and a second adjacent pixels in the first row and a third pixel adjacent to said first and second pixels in the second row form a delta structure, each of the three vertices of the delta structure being a center of the first, second and third pixels, respectively.

22 The liquid crystal display device of claim 21, wherein the distances between the centers of the first, second, and third pixels are substantially equal.